Bulk built in current sensors for single event transient detection in deep-submicron technologies

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Abstract

As device dimensions are scaled down, single event transients (SET) are increasingly affecting the reliability of integrated circuits. An SET is a transient voltage perturbation caused by an energetic particle strike at the semiconductor. This work studies the applicability of bulk built in current sensors (bulk-BICS) for SET detection in deep-submicron technologies. The bulk-BICS detects the transient current generated by the impact of an energetic particle at a sensitive circuit node. The efficiency and applicability of this approach to SET detection is demonstrated through device and circuit level simulations.

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1. Introduction

Aiming to increase circuit performance, as well as to integrate more functional units into the same silicon area, scaling leads to integrated circuits made of ever shrinking devices. Power supply is also scaled down. As a consequence, the amount of electrical charge used to store information is ever decreasing. This decrease in electrical charge used to store information has made integrated circuits more susceptible to transients caused by energetic particle strikes. If an energetic particle strikes a sensitive region in a semiconductor device, the resulting electron-hole pair generation injects electrical charge into the struck node. As the charge used to store information decreases, the electrical impact of the charge injected by the particle hit increases. The electrical charge injection changes the electrical voltage at the struck node. This temporary voltage disturbance at a circuit node is called a single event transient (SET). In digital circuits, if the voltage disturbance is high enough, it may be interpreted as a valid logical signal and be propagated through the logical path. If it propagates to a latch or other memory element, it may change the results of a computation.

With decreasing device dimensions in modern technologies, SETs become a concern not only in avionics and aerospace environments, but also at sea level [1–4]. At sea level there are two major radiation sources that can cause SET. The first source is atmospheric neutrons and protons, which may create secondary ions when interacting with atoms in the target device. The second source is alpha particles emitted by radioactive impurities present in the device itself or in the packaging materials. At aircraft altitude or space environment cosmic rays (heavy ions) are also a concern. It is identified by the international technology roadmap for semiconductors (ITRS), that beyond the 90 nm node, single event transients severely impact field-level product reliability, not only for embedded memory, but for logic as well [1].

As a consequence, efficient techniques to improve the reliability of integrated circuits against radiation effects are demanded.

In previous work a new approach based on built in current sensors (BICS) able to detect SETs in integrated circuits was proposed [2]. In that work the electrical behavior of the struck device was studied by electrical simulation.
only. In the current work the behavior of the struck transistor is studied by detailed device simulation, thus validating the proposed approach. Furthermore, the impact of scaling is also studied. It is shown that bulk built in current sensors (bulk-BICS) are an efficient solution for SET detection.

2. Bulk built in current sensors

For energetic particle strikes at integrated circuits, the critical regions are the reverse biased pn-junctions [3,4]. A particle hit at a reverse biased pn-junction causes a transient current, changing the voltage at the struck node. This voltage change may be interpreted as a valid signal in the circuit, leading to a transient fault.

Built in current sensors have been used for monitoring on-chip current variations due to permanent faults, as for instance stuck at faults [5,6]. For transient fault detection, related works have presented asynchronous BICS able to detect single event upsets (SEUs) in memories [7]. In this case, the BICS is placed on the power lines of a memory. Monitoring the current in the supply rails may be an efficient solution for sequential circuits. However, this solution does not work properly for combinational logic, because BICS connected to the power lines cannot efficiently differentiate SETs from internal signals propagating through the logic.

In order to enhance the applicability of the BICS approach and more efficiently detect SETs in integrated circuits, we propose a new approach able to detect transient faults based on bulk built in current sensors (bulk-BICS) [2]. In this method, a BICS is connected to the design bulk of the transistors, which increases the BICS efficiency to detect any discrepancy in the circuit internal current that may occur during a particle strike. Since under normal circuit operation the bulk current is very small if compared to the current generated by a particle strike, this approach allows the bulk-BICS to distinguish SETs from internal logic signals and consequently detect them. As a consequence, the bulk-BICS may be used to detect transient faults in digital combinatorial logic and mixed signal circuits, as well as in memories.

A simple bulk-BICS design is depicted in Fig. 1. This simple design will be used to study the bulk-BICS detection mechanism in the next section. An advantage of this design is its negligible static power consumption, a key feature for VLSI. This bulk-BICS detects a SET due to an energetic particle strike at the reverse biased drain junction of PMOS transistors in the off state, and will be called pBICS through this work. The body-ties of the PMOS transistors being monitored are connected to \( V_{DD} \) through transistor M1 of the bulk-BICS. To ensure proper connection of the body-ties to \( V_{DD} \), the PMOS transistor M1 has a large \( W/L \) ratio. \( L \) is the channel length and \( W \) the channel width. The PMOS transistor M2 also has a large \( W/L \) ratio, while the NMOS transistor M3 has a small \( W/L \) ratio. Under normal operation (no particle strike) the current flowing through M1 is negligible, and the gate of M2 is at \( V_{DD} \). As a consequence, the output Out-P of the bulk-BICS is at logic zero. If a particle strike occurs, current flows through M1, and the gate voltage of M2 slightly drops. The bulk-BICS amplifies this voltage change, and the output voltage at Out-P rises, changing its value from logic zero to logic one. Out-P may be latched and used as a flag to signal the occurrence of a SET. Error handling techniques may then be implemented at the circuit or system level, aiming to avoid that a SET turns into a faulty behavior.

A similar design (nBICS) may be used to detect particle strikes at the drain of NMOS transistors in the off state [2]. Circuit and device simulations for both cases (strikes at NMOS and PMOS transistors) lead to equivalent results. To keep the paper compact, only the simulation results for particle hits at the drain of a PMOS transistor in the off state are shown here.

3. Device and circuit level simulations

The single event transients are simulated using the synopsys taurus medici package [8]. Mixed mode (level) simulations are performed using the circuit analysis advanced application module. The charge collection and current generation mechanism are simulated in three-dimensions at the device level, while the bulk-BICS response is simulated at the circuit level.

To simulate the environment of the transistor operating in a real circuit, the struck transistor is simulated as being part of an inverter. It is the PMOS transistor of a CMOS inverter, driving another inverter. It is the PMOS transistor labeled M1 in Fig. 2. This circuit is simulated in two different technologies, as described below.

In this case study, the input of the first inverter is connected to \( V_{DD} \). Hence, the gate contact of M1 is fixed at \( V_{DD} \). The source contact of M1 is also connected to \( V_{DD} \). The drain contact of M1 is connected to the output node of the inverter. The struck transistor is then in the off state. The body-tie of M1 is connected to \( V_{DD} \) through the bulk-BICS depicted in Fig. 1. These voltages reverse bias the struck drain–substrate junction.
Two different technologies are simulated as case studies. For the first technology, the PMOS transistor simulated at the device level has peak source/drain doping equal to $10^{20}$/cm³. The substrate doping is $2 \times 10^{18}$/cm³. The peak doping of the n-type implant for the body-tie contact is also $10^{20}$/cm³. The junction depths at the source and drain contact are approximately 75 nm. The source/drain extension (LDD) junction depth at the channel end is approximately 25 nm. The polysilicon gate length is 90 nm, and the physical (metallurgical) channel length is approximately 65 nm. The simulations are carried out with power supply VDD equal to 1.2 V. The threshold voltages of NMOS and PMOS transistors are 0.23 and 0.25 V, respectively. These parameters are in agreement with the parameters for a typical 90 nm technology for ASIC’s, after data made publicly available by the ITRS [1], as well as the well tempered transistor website [12].

For the second technology, the PMOS transistor simulated at the device level has peak source/drain doping equal to approximately $2 \times 10^{20}$/cm³. The substrate doping is $3 \times 10^{19}$/cm³. The peak doping of the n-type implant for the body-tie contact is also nearly $2 \times 10^{20}$/cm³. The junction depths at the source and drain contact are approximately 55 nm. The source/drain extension (LDD) junction depth at the channel end is approximately 17 nm. The polysilicon gate length is 65 nm, and the physical (metallurgical) channel length is approximately 40 nm. The simulations are carried out with power supply VDD equal to 1.0 V. The threshold voltages of NMOS and PMOS transistors are 0.22 and −0.23 V, respectively. These parameters are in agreement with the parameters for a typical 65 nm technology for ASIC’s, after data made publicly available by the ITRS [1].

A cross section of the struck PMOS transistor is depicted in Fig. 3. This picture refers to the simulations performed for the 90 nm technology node. A three-dimensional view is show in Fig. 6. The channel width ($W$) is equal to 400 nm.

To study the bulk-BICS detection mechanism, a 5.5 MeV alpha particle passing through the drain of the p-channel MOSFET is simulated in three-dimensions. The charge generation rate versus depth of penetration of the alpha particle is obtained from [9]. The particle strikes at the reverse biased drain junction, at position $x = 0.05$ μm and $z = 0.05$ μm, perpendicular to the silicon surface. During the upset process, the conductive charge track generated by the passage of the energetic particle temporarily short circuits the drain–substrate junction and pulls the drain up to the higher potential of the substrate. This voltage change at the drain node is known as single event transient at the circuit level, and may lead to circuit faulty behavior. The first 300 picoseconds (ps) of the transient response are simulated. The particle strike occurs at time $t = 0$.

Fig. 4 shows the voltage at the drain contact of the struck transistor, from $t = 0$ to 80 ps. It can be seen that a 5.5 MeV alpha particle induces a wider transient in the 65 nm technology, if compared to the 90 nm technology. The charge generation rate versus depth of penetration of the alpha particle is obtained from [9].

The particle strikes at the reverse biased drain junction, at position $x = 0.05$ μm and $z = 0.05$ μm, perpendicular to the silicon surface. During the upset process, the conductive charge track generated by the passage of the energetic particle temporarily short circuits the drain–substrate junction and pulls the drain up to the higher potential of the substrate. This voltage change at the drain node is known as single event transient at the circuit level, and may lead to circuit faulty behavior. The first 300 picoseconds (ps) of the transient response are simulated. The particle strike occurs at time $t = 0$.

Fig. 5 depicts the current at the drain and source terminals of the struck transistor, as well as the body-tie current, from $t = 0$ to 60 ps, for the 90 nm technology. The large spike in drain current (approximately 0.28 mA) is due to drift collection. The drift collection process is quickly extinguished (at about 15 ps) as all the charge in the depletion region is collected. Fig. 4 shows that the voltage at the drain terminal reaches a maximum (of about 60% of VDD for the 90 nm technology and VDD for the 65 nm technology) and slowly starts to return to ground, as the conductive channel between drain and substrate is extinguished and the drain circuit node is pulled down to ground.
through the NMOS transistor (M2) of the first inverter (see Fig. 2).

A funneling behavior [10,11] can be seen by examining the potential contours, as shown in Fig. 6, which refers to the 90 nm technology. For the 65 nm technology the results are equivalent. The simulation domain extends 2 \( \mu \text{m} \) into the silicon bulk (\( y \)-axis), although only the top 1 \( \mu \text{m} \) is plot. Before the ion strikes, the equipotentials are parallel to the drain junction. The figure depicts the situation at 6 ps after the alpha particle strike. The equipotentials extend into the substrate due to the voltage drop along the charge column. The funneling reaches its peak at around 6 ps, approximately the same time at which the drain current reaches its peak. Afterwards, the funnel starts to collapse and the drift current starts to decrease, as charge is swept from the depletion region at the drain.

Fig. 4. Voltage at the drain contact of the struck PMOS transistor. Circles (\( \bullet \)) are the simulation results for the 90 nm technology, squares (\( \square \)) correspond to the simulation results for the 65 nm technology. For the 90 nm technology the single event transient reaches a peak voltage of approximately 60\% of \( V_{\text{DD}} \). For the 65 nm technology the single event transient reaches \( V_{\text{DD}} \).

Fig. 5. Current at the drain and source contacts of the struck transistor, as well as at the body-tie. Squares (\( \blacksquare \)): drain current, triangles (\( \triangle \)): body-tie current, circles (\( \bullet \)): source current.

After 25 ps the depletion region at the drain is restored and only diffusion charge collection is occurring. The simulation time of 300 ps is sufficient to resolve the drift component of the charge collection process. At the end of the simulation time, there is only a small current of a few microamperes at the drain terminal, due to diffusion charge collection.

Fig. 7 depicts the bulk-BICS transient response, from \( t = 0 \) to 80 ps. The voltage at the bulk-BICS output
(Out-P) is plotted, for both the 65 nm and the 90 nm technology. In both cases, the output of the bulk-BICS crosses the logical threshold, changing its output state from logical zero to logical one. Since the transistor M2 of the pBICS has much larger W/L ratio than M3, the output quickly changes from logical zero to logical one. After reaching its peak value, the output slowly returns to zero, due to the current conducted through M3. Out-P may be latched, for instance using an asynchronous latch, and used as a flag to signal the occurrence of a SET. Techniques to mitigate the effects of a SET may then be implemented at the circuit or at the system level, improving product reliability. For instance, if the bulk-BICS is used to monitor the circuitry of a microprocessor with recomputing and pipeline refreshing capabilities, Out-P may be used to signal the need for recomputation or pipeline refreshing. The bulk-BICS approach may help improving high-level fault-tolerance methods based on fault detection and correction.

To verify the impact of body-tie spacing on bulk-BICS detection, the distance between body-tie and struck transistor was varied. If the body-tie is placed 5 µm apart from the struck transistor, the peak current at the body-tie decreases by about 10%, and the bulk-BICS properly detects the particle hit. The total charge injected at the body-tie contact (integration of current over time) changes less than 5%. The change in the current and voltage waveforms at the drain contact is negligible.

A single bulk-BICS can be used to monitor several transistors. This can be done by connecting the input of the bulk-BICS (“to body-tie” contact) to several body-ties. However, since this increases the capacitance at this node, there is a limit for the maximum number of transistors that can be monitored by a single bulk-BICS, as discussed in [2]. The maximum number of transistors that can be monitored by a single bulk-BICS depends on technology node and bulk-BICS design. In [2], two bulk-BICS are used to detect SETs in up to 128 SRAM memory cells.

The impact of scaling on circuit behavior and bulk-BICS detection was also studied. With scaling, node capacitances and supply voltages decrease, and integrated circuits become susceptible to SETs due to strikes by lower energy particles. The transient pulse width increases for alpha particles striking at sensitive nodes in the 65 nm technology, if compared to the 90 nm technology, as seen in Fig. 4. The transient pulse width is the time during which the voltage change (perturbation) at the node is greater than VDD/2. For both technologies, the charge deposited by the alpha particle is nearly the same, leading to an increased transient pulse in the 65 nm technology. This increase in pulse width is related to the decrease in power supply and node capacitance, which leads to a smaller charge stored at the struck circuit node. In our case study circuit, the node capacitance is dominated by the drain junction capacitance and the capacitive loading due to the inverter driven by the struck node. With scaling, these capacitances are diminished.

It is important to note that with scaling not only the duration of the transient pulse increases. The delays of the logic gates also decrease, leading to shorter clock cycles. As a consequence, the transient pulse lasts for a longer fraction of the clock cycle. Longer transients may more easily be propagated through the logic chain. Increasing clock frequencies also mean that there are more latching clock edges to capture a transient pulse. This increases the latching probability of a transient. Hence, it can be concluded that scaling leads to higher vulnerability for future technologies.

As can be seen from Fig. 7, with scaling the bulk-BICS response becomes faster and its sensitivity is expected to increase. For the 65 nm technology, the same alpha particle hit causes a larger change at the bulk-BICS output, if compared to the 90 nm technology. It is important to note that the sensitivity of the bulk-BICS can be further increased by increasing the channel length L of transistor M3 of the bulk-BICS, for instance. The bulk-BICS sensitivity may be calibrated according to the energy of the particles of interest.

Particle hits by ions of higher and lower linear energy transfer (LET) have also been simulated, using the mixed mode simulation methodology described here. Particles that deposit more charge result in an increased voltage perturbation at the drain terminal, and induce a higher body-tie current. The capacitive and resistive loading effects at the drain contact have also been analyzed. As discussed in [2], the bulk-BICS sensitivity may be adjusted by proper sizing of transistors M1, M2 and M3 of the bulk-BICS, or by using improved bulk-BICS designs. The mixed mode simulations run confirm that the bulk-BICS approach is efficient in detecting single event transients.

4. Conclusion

The efficiency of the bulk built in current sensor approach for single event transient detection is validated by device simulation. It is shown that the bulk-BICS properly detects the energetic particle strike, presenting an efficient technique to improve the reliability of integrated circuits against radiation effects. The impact of scaling on circuit and bulk-BICS behavior is also discussed.

Ongoing work is focusing on the design, fabrication and test of a chip with an integrated bulk-BICS under energetic particle bombardment (irradiation).

References


