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Sub 1 V CMOS bandgap reference design techniques: a survey

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Abstract This paper presents a review of constraints, limitation factors and challenges to implement sub 1 V CMOS bandgap voltage reference (BVR) circuits in today's and future submicron technology. Moreover, we provide insight analysis of BVR circuit architectures a designer can relay upon when building CMOS voltage reference.

Keywords Low-voltage CMOS bandgap voltage reference · Deep submicron · Operational amplifier · Dynamic threshold MOSFET

1 Introduction

Bandgap voltage references (BVR) are circuits that provide a temperature and supply insensitive output voltage. Voltage references are among the most important building blocks in analog circuits and are used in dynamic random access memory (DRAM), flash memories, power supply generation, DC bias voltage, current sources, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs). In addition, the performances and precision of coders and/or decoders, as well as the conversion accuracy of signal processing blocks in data converters systems are strongly dependent on the accuracy of the reference voltage. Traditionally, the output reference voltage has always been approximately equal to the intrinsic bandgap voltage of the semiconductor material used, the silicon for instance. In bandgap reference, an output voltage with low sensitivity is obtained as the sum of a voltage that is proportional to absolute temperature (PTAT) and a voltage with negative temperature coefficient, which is complementary to absolute temperature (CTAT). The PTAT voltage is generated by taking the difference in the base-emitter voltages of two bipolar transistors. The CTAT voltage is usually obtained from the voltage across a forward biased p–n junction or the base-emitter voltage (V_{BE}) of a diode connected bipolar junction transistor (BJT) as illustrated in Fig. 1. The term V_T indicated in this figure is the thermal voltage described by Eq. 1, where k is the Boltzmann constant, q is the electron charge and T is the temperature.

$$V_T = \frac{kT}{q} \tag{1}$$

In CMOS technology, parasitic vertical BJT transistors formed in p- or n-well are used to implement BVR circuits. The key parameters that specify the performance of BVR circuits are expressed in terms of initial accuracy, temperature insensitivity, supply current or power consumption. Furthermore, immunity to power supply noise, robustness to process variation, reliability, long term drift and temperature hysteresis are among additional key

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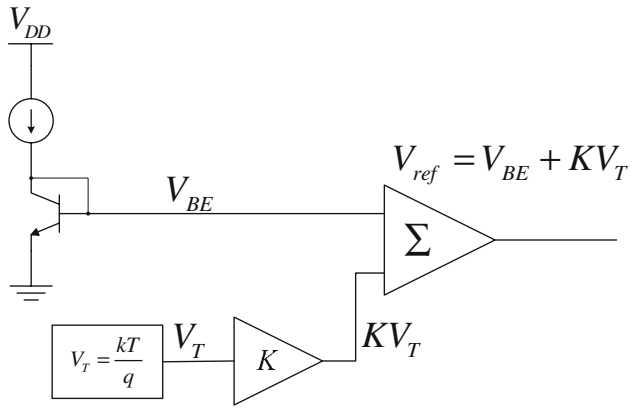

Fig. 1 Block diagram of a bandgap voltage reference

performances parameters. The initial accuracy of voltage reference is referred as the output voltage at room temperature and provides the starting point for most of the other specifications. The temperature coefficient represents the deviation of the output voltage because of changes in the ambient or package temperature. The temperature hysteresis outlines the amount of variation of the output voltage after a cycle of temperature change. When the references experience a temperature change and return to the initial temperature, they frequently do not have the same initial output voltage. This variation is caused by the mechanical stress applied to the chip. The mechanical stress is due to the difference in thermal coefficient of expansion between the silicon chip, package and PC board. As this type of error depends on temperature excursion, reference design and type of package, it is difficult to correct and it can considerably damages the reference accuracy. The stability is a measure of the variation in the output voltage after a long period of operation. The desired performances of BVR circuits and systems are precise initial accuracy, strong temperature insensitivity, low current or power consumption, and low noise.

This tutorial presents a review of state-of-the-art design techniques to implement sub 1 V BVR circuits that generate stable reference regardless of both temperature and supply voltage variation. Reduced power supply voltage is normally not an advantage for voltage reference design and a low supply voltage may require some special circuit techniques. Technology scaling and demand for low power applications lead to lower supply voltages, below the intrinsic bandgap voltage. An overview of the limitation factors affecting the performance of BVR circuits is presented in Sect. 2. Section 3 is a review of the state-of-the-art design techniques that have been recently proposed to implement sub 1 V voltage reference. The summary is presented in Sect. 4.

2 Design challenges of sub 1 V CMOS bandgap references

Reference voltage generators are required to be stabilized over process, voltage and temperature variations, and also to be implemented without modification of fabrication process. The conventional output voltage of BVR circuit is 1.25 V, which is nearly the same voltage as the bandgap of silicon. This fixed output voltage of 1.25 V limits the minimum supply voltage (V_{DD}) operation. In addition, since the main popular trends in the design of BVR circuits rely on the usage of an operational amplifier (opamp) in the PTAT current generation loop, the offset of the opamp greatly affects the accuracy of the BVR circuit. Moreover, the currents mirrors mismatch, the resistors mismatch, the transistors mismatch, the emitter-base voltage (V_{EB}) spread, and the package shift are among the main dominant sources of errors affecting the performance of BVR [1–6]. However, BVR circuit performance is limited by its absolute accuracy (how close the output can be set to a desired value at nominal operating condition) and its relative error (how much the voltage varies from the nominal value over the full range of operating condition). Moreover, for precision applications such as in data converter systems, the relative error of a voltage reference ultimately determines how useful the circuit will be. The relative stability of a BVR circuit is determined by the temperature coefficient of the reference over the operating temperature range, the power supply noise rejection (PSR) over the operating voltage range, the load regulation over the range of output load impedances, and the peak-to-peak output noise generated by the intrinsic noise sources of the circuit [1].

2.1 Operational amplifier offset

The inherent random offset in MOSFETs transistors gate source voltages which arises from the mismatches in threshold voltages, *W*/*L* ratios, electron and hole mobilities, results into opamp offset. The latter is directly superimposed onto the resistor R_{PTAT}, in addition to the desired difference of the emitter-base voltage (ΔV_{EB}), and is amplified by the same factor. Therefore, the opamp offset voltage is the prevailing source of process induced error in CMOS BVR architecture similar to Fig. 2.

2.2 Current mirror mismatch

When referring to Fig. 2, any mismatch in the required current ratio of the current mirror formed by PMOS transistors M_1–M_2, would result in a difference in the current flowing through the BJT transistors Q_1–Q_2. Deviation in the current mirror are due to isolated and/or combined effects of mismatch in the *W*/*L* ratio, threshold voltage

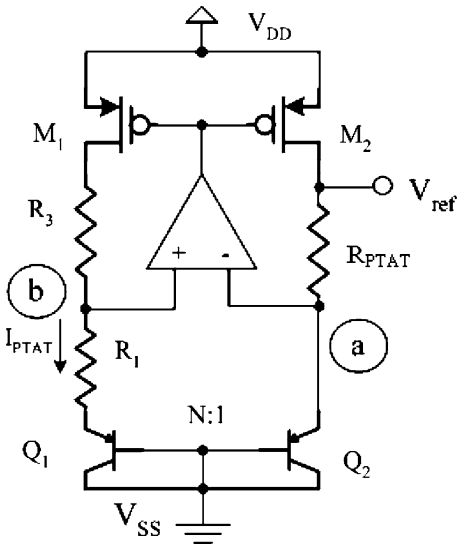

Fig. 2 Typical CMOS bandgap voltage reference

mismatch, channel length modulation effects of MOS transistors, resistors mismatch. Moreover, for submicron technologies, the short channel effects (SCE), the drain induced barrier lowering effects (DIBL), and some additional stress such as the length of oxide definition (LOD) effect on matched devices would contribute to additional mismatch. These errors can be mitigate through layout techniques such as the common centroid and compact layout, dummy devices at no additional cost or by laser trimming, which is a more expensive offset correction technique. Another example of practice to improve the current source matching is the addition of resistor R_3, otherwise devices M_1 and M_2 would have different drain-source voltages.

2.3 Resistor mismatch and resistor tolerance

Random process induced variation of the resistor value directly affect the V_{EB} and consequently the PTAT voltage. The induced error in the output voltage (V_{REF}) of BVR circuit is given by Eq. 2

$$\Delta V_{REF} = -V_T \delta_{RA} \tag{2}$$

where δ_{RA} is the fractional deviation of the resistors from their nominal values [2]. Resistors mismatch affect the PTAT voltage as given by Eq. 3

$$\Delta V_{REF} = V_{PTAT} \delta_{RR} \tag{3}$$

where δ_{RR} is the mismatch in the resistors. For example, considering the topology shown in Fig. 2, the PTAT current and the output voltage are given by (4) and (5). If the resistor R_1 has a variation of $\pm\ \Delta R_1$, the PTAT current will suffer a variation of ΔI described by Eq. 6—where α is the term that multiplies V_T. This error will be amplified by R_{PTAT} at the output voltage, then generating an error (ΔV_{REF}) equal to $-V_T \times \delta_{RA}$, where δ_{RA} is given by $-\alpha \times R_{PTAT}$.

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_1} = \frac{V_T \times \ln(N)}{R_1} \tag{4}$$

$$V_{REF} = V_{BE_2} + I_{PTAT} \times R_{PTAT} \tag{5}$$

$$\Delta I_{PTAT} = \frac{\Delta R_1 \times \ln(N)}{R_1 \times (R_1 \pm \Delta R_1)} \times V_T = \alpha \times V_T \tag{6}$$

Layout techniques are the most efficient and non-costly means to reduce the effect the resistors mismatch induced errors. Especially, layout of resistors should be laid in a square like structure and in a common centroid fashion. Resistors material are preferably in polysilicon since its offer the minimum separation of resistor fingers. Thus providing a compact layout and better matching. In addition, a polysilicon resistor has a smaller resistance spread over temperature than diffusion resistor. Also, when available, lightly doped polysilicon is a better choice since it has a negative temperature coefficient.

2.4 Transistor mismatch

The output voltage of traditional BVR circuit is basically the sum of an emitter-base voltage and a scale value of the thermal voltage. Any spread in V_{EB} would have a large effect in the relative error of the BVR. In addition, any deviation in the area of transistors Q_1–Q_2 in Fig. 2, would result in an error (ΔV_{REF}), and is given by

$$\Delta V_{REF} = \frac{1}{\ln(N)}(V_T + V_{PTAT})\delta_{PNP} \tag{7}$$

where δ_{PNP} is the fractional error in the transistors area ratio [2–4].

2.5 Package induced offset

Package induced voltage shift is the difference between the voltage reference caused by the local and die-wide mechanical stress of a package in its encapsulated integrated circuit (IC). This shift is caused by the stress imposed by the package on the die surface. The dominant factor is due to the difference in the thermal coefficient of expansion of the silicon die and the plastic mold. The plastic package transfers an increasing stress to the chip as the package cools from molding to ambient temperature. A common technique to reduce the effect of this error is to use silica fillers that reduce the thermal expansion and prevent destructive effects like corner and passivation layer cracking as well as metal line shifts. Also, thick elastic film layer between the plastic mold and the die surface can absorb some of the stress from the plastic mold [6].

3 Design of sub 1 V CMOS bandgap voltage references

Design of high performance analog IC's circuits operating at low supply voltages has been gaining increasing importance in the last decade, especially for applications such as medical electronic implantable devices, as well as battery powered electronic hand-held devices, and systems. Furthermore, the increasing use of mobile electronic products has directed the industry towards reducing dissipated power, especially for analog and mixed signal circuits. Therefore, BVR circuits, which are the main building blocks of analog circuit, are required to target sub 1 V operation, while generating temperature insensitive output voltage under supply voltage lower than the semiconductor material bandgap voltage. Even if the output reference voltage is no longer equal to the silicon bandgap voltage, most designers still use the name "CMOS Bandgap Voltage Reference" instead of "CMOS Voltage Reference or CMOS Current Reference" to differentiate circuits that use the same idea of compensating the dependence of the CTAT with the PTAT. A basic architecture of bandgap voltage reference using a transimpedance amplifier is shown in Fig. 3, and is composed of PMOS transistors M_1 and M_2, vertical BJT transistors Q_1 and Q_2, a transimpedance amplifier and two resistors R_1 and R_2 [7]. The operational amplifier (opamp) forces the two nodes "a" and "b" to have the same potential, thus generating a PTAT voltage across the resistor R_1 as the difference of the V_{EB} of Q_1 and Q_2. The proposed circuit is used to generate a reference voltage (V_{REF}) of 1 V with an untrimmed relative error (V_{error}) of 10 mV. This relative error becomes $V_{error} = 3$ mV after trimming the resistor R_1 over a temperature range of 0–100°C. The authors have demonstrate

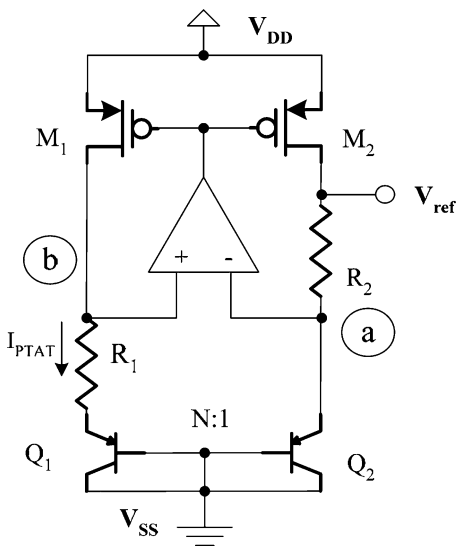

Fig. 3 Bandgap voltage reference using a transimpedance amplifier proposed by Jiang et al. [1]

that one of the limitations of implementing opamp based sub 1 V BVR circuits arise from the limitation imposed by the input common mode voltage of the opamp.

Traditionally, designers of BVR circuits have mainly focused on generating insensitive output voltage more or less equal to the bandgap voltage of the semiconductor material used. The main limitation in implementing sub 1 V BVR circuits is that the bandgap voltage of silicon is around 1.25 V. Moreover, for BVR circuits that use opamp, additional limitation arises from the fact that the input common mode of the opamp used in the PTAT current generation loop has to be in the order of one base-emitter voltage. Several techniques have been proposed to overcome these limitations to implement sub 1 V bandgap voltage reference circuits in CMOS technology. The resistive subdivision technique combined with the used of native transistors [8, 9], are among the schemes that have been proposed to scale down the 1.25 V output reference voltage. Some design techniques have consisted of implementing opamp with low input common mode voltage level by the use of BiCMOs technology [10]. In standard CMOS technology, the technique of partially forward biasing the source bulk junction of PMOS transistors while making sure that the opamp is maintained in the high gain region have been proposed [11, 12]. Other design techniques of implementing sub 1 V BVR circuits are based on the usage of subthreshold transistors [12, 13], in order to take advantage of their low threshold voltage capability, or by a combine usage of depletion mode and enhancement mode transistors [14], or by taking advantage of the difference in the gate work function material of transistors having different doping level and type [15]. Additionally, dynamic threshold MOSFET (DTMOS) [16] have also been proposed to implement sub 1 V BVR circuits. Review of reliable sub 1 V opamp design techniques has been previously presented in [17]. Moreover, noise performance of BVR circuits is a very important requirement that is affected when the supply voltage and current consumption are to be low. However, designers can use the chopper stabilizing technique to achieve a trade off between supply voltage and noise performance [18].

3.1 Sub 1 V bandgap circuits based on resistive division technique

Neuteboom et al. [8], propose the BVR circuit illustrated in Fig. 4, which is based on the resistive division technique and provide an output voltage lower than the bandgap voltage of the silicon. The BVR circuit makes use of three vertical PNP transistors with emitter ratio of N. The opamp controls the emitter current and maintains a ΔV_{EB} across the resistor R_1 in the PTAT current generation loop. Operation under low supply voltage operation condition is

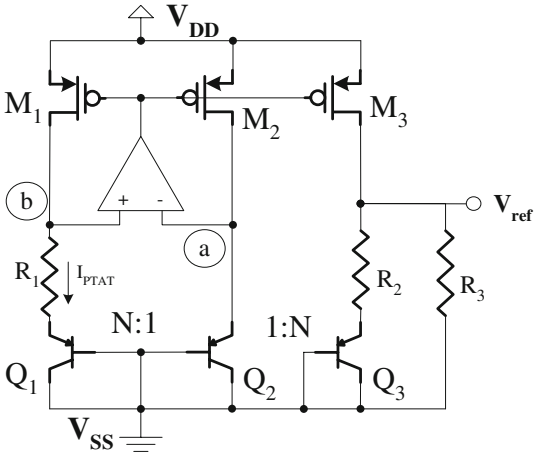

Fig. 4 Bandgap voltage reference circuit proposed by Neuteboom et al. [8]

achieved by connecting the resistor R_3 across the bandgap reference, and the resulting output voltage becomes a fraction of the bandgap voltage which is given by

$$V_{\mathrm{REF}} = \frac{R_3}{R_2 + R_3}(V_{\mathrm{EB}} + I_{\mathrm{PTAT}} R_2) \tag{8}$$

which can be scaled to any value. A fraction of the bandgap voltage is obtained by proper choice of resistors R_2 and R_3. The proposed circuit achieves an output voltage of 0.67 V, under a minimum supply voltage of 0.9 V. Similar technique to generate output voltage lower than the material bandgap have been used by Banba et al. [9], and Malcovati et al. [10]. Banba et al. proposed the CMOS BVR circuit illustrated on Fig. 5. In this BVR circuit, two currents that are proportional to voltages at nodes a and b are generated. The opamp is used to force the two voltages V_a and V_b to be equal thus producing a current in the nominally equal resistors R_{2A} and R_{2B} proportional to V_{EB}.

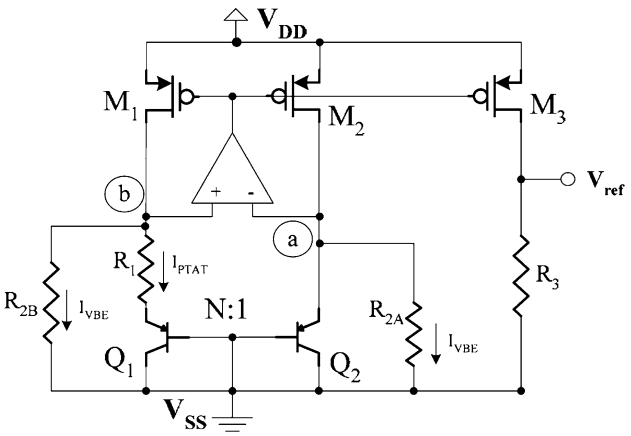

Fig. 5 Bandgap voltage reference architecture proposed by Banba et al. [9]

As a result the current in the PMOS transistors M_1, M_2 and M_3 ($I_1 = I_2 = I_3$) is given by

$$I_1 = \frac{V_T \ln(N)}{R_1} + \frac{V_{\mathrm{EB}}}{R_{2\mathrm{A}}} \tag{9}$$

and the output voltage is then given by Eq. 10, where N is the emitter area ratio of the two diode connected bipolar transistors Q_1 and Q_2.

$$V_{\mathrm{REF}} = \frac{R_3}{R_{2\mathrm{A}}}\left[V_T \frac{R_{2\mathrm{A}}}{R_1}\ln(N) + V_{\mathrm{EB}_2}\right] \tag{10}$$

The theoretical minimum supply voltage for this circuit architecture is $V_{\mathrm{DD(min)}} = V_{\mathrm{EB}} + V_{\mathrm{thp}}$. The compensation of the temperature coefficients of the thermal voltage V_T and V_{EB} is achieved by choosing the values of N and of the $R_{2\mathrm{A}}/R_1$ ratio which satisfy

$$\frac{R_{2\mathrm{A}} \ln(N)}{R_1} = 22 \tag{11}$$

For proper sub 1 V operation, the authors proposed an opamp circuit based on native MOS transistors which are not always available in standard digital CMOS technology process. Moreover, these BVR circuits require the usage of parasitic vertical PNP transistors included in CMOS process, but which are not very well characterized. The vertical PNP transistors are process dependent and offer limited robustness to process variation as the doping gradient, process parameters vary a lot within transistors of the same die. Some design advantages, such as enhanced insensitivity to ripple in the power supply and/or better power supply rejection ratio (PSRR) performance could be obtained using cascode devices in the current mirror but at the expense of an increased of the minimum power supply.

The opamp used in BVR circuits are required to be fully operational under sub 1 V condition. Since the output node drives p-channel current sources, and considering that $|V_{\mathrm{th}},p| = 0.7$, the output quiescent voltage should be maintained to be around 0.15–0.2 V in order to maintain the PMOS transistors current mirror in strong inversion. Moreover, their input common mode voltage should be maintained at value at least equal to one emitter-base voltage of 0.65 V, even though the emitter-based voltage of BJT decreases to value around 0.45 V when the temperature is increased up to 100°C. Similar BVR core circuit has been proposed by Malcovati et al. [10], and is depicted in Fig. 6. The later enables designers to overcome the limitation of the low input common mode voltage requirement for the opamp and enhance the implementation of a sub 1 V BVR circuit by using the BiCMOS process technology. The proposed BVR circuit has two stable operating points and requires a start-up circuit to prevent operation in the undesired operation point. In addition, the circuit compensates for first order temperature

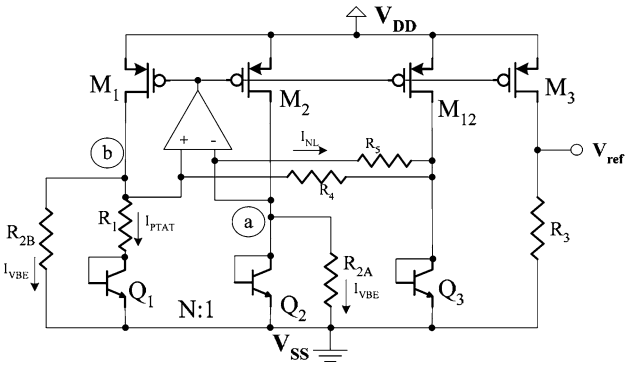

Fig. 6 Low voltage BiCMOS bandgap with curvature compensation proposed by Malcovati et al. [10]

dependence only as outlined in Eq. 12. The V_{BE} of a BJT does not change linearly with temperature but according to the relationship given by

$$V_{BE}(T) = V_{BG} - (V_{BG} - V_{BE_0})\frac{T}{T_0} - (\eta - \alpha)V_T \ln\frac{T}{T_0} \quad (12)$$

where η depends on the bipolar structure and is around 4, while α equals 1 if the current in the BJT is PTAT and goes to 0 when the current is temperature independent. The current in the PMOS transistors of the bandgap circuit is copied by using transistor M_{12} and injected into a diode connected BJT transistor Q_3. A V_{BE} with $\alpha = 0$ is produced across Q_3. The difference between $V_{BE,Q_3}(T)$ and $V_{BE,Q_{1,2}}(T)$ leads to a voltage proportional to the nonlinear term of Eq. 12

$$V_{NL} \cong V_{BE,Q_3}(T) - V_{BE,Q_{1,2}}(T) = V_T \ln\frac{T}{T_0} \quad (13)$$

The opamp input stage is based on two grounded PNP transistors as shown in Fig. 7. The bias current in the differential pair of the opamp is a replica of the current in the diode connected BJT of the bandgap structure, since transistor Q_1 of the bandgap and Q_3 of the input stage of the opamp form a current mirror. This enables the designer to overcome the need of having current source in the input stage of the differential amplifier that required at least one saturation voltage to operate properly. The current signal generated by the input differential pair Q_3–Q_4 is folded and collected by diodes connected MOS transistors (M_6 and M_7). The resulting differential gain becomes

$$A_d = \frac{g_{m,BJT}}{g_{m,MOS}} = \frac{I_{BJT}/V_T}{2I_{MOS}/(V_{GS} - V_{th,n})} \quad (14)$$

where the suffix BJT refers to the input BJT and the suffix MOS refers to the diode loads M_6 and M_7. Using $I_{BJT} = 4\,I_{MOS}$ the gain obtained is 8 while having a fully symmetrical input and a practically zero systematic offset. The second stage is only a push-pull circuit. Curvature compensation is achieved by subtracting, from both I_1 and I_2, a current proportional to V_{NL}. This is obtained by adding nominally equal resistors R_4 and R_5, which drain from M_1 and M_2 the required current (I_{NL}) as shown in Fig. 6, and leading to output voltage of

$$V_{REF} = \frac{R_3}{R_{2A}}\left(\frac{R_{2A}\ln(N)}{R_1}V_T + V_{BE} + \frac{R_{2A}}{R_{4,5}}V_{NL}\right) \quad (15)$$

The proposed BVR architecture achieves an output voltage of 0.536 V with a temperature coefficient of 7.5 ppm/K when the temperature changes from 0°C to 80°C, and a voltage supply coefficient of 212 ppm/V.

Ker et al. [11], proposed a BVR circuit that provide a fraction of the bandgap voltage by mean of resistive division to reduce the input common mode voltage requirement of the opamp, without using low threshold devices as illustrated on Fig. 8. The proposed BVR circuit also exploits the alternate connection technique of the opamp input stage by connecting it to nodes V_1 and V_2 instead of nodes a and b as was done in previous works. We should recall that the main idea presented by Leung et al. and Ker et al., being to provide alternate connection points of the

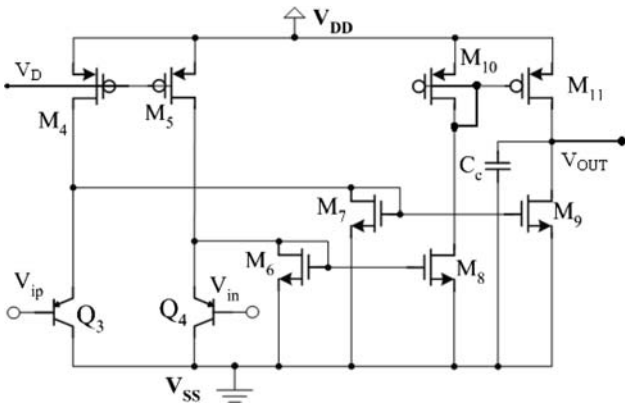

Fig. 7 Schematic of the two-stage opamp used in the voltage reference proposed by Malcovati et al. [10]

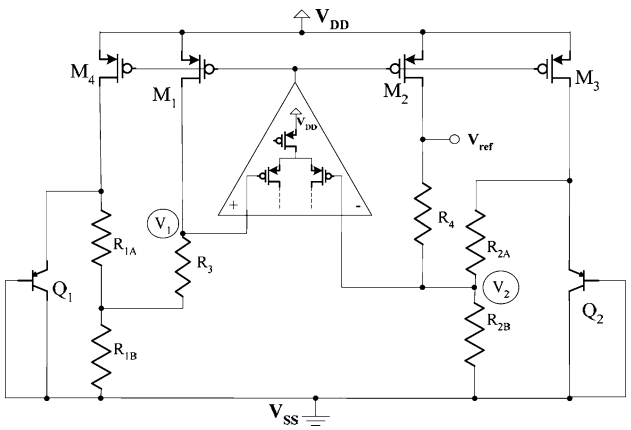

Fig. 8 Bandgap voltage reference without using low threshold devices proposed by Ker et al. [11]

opamp input stage. The proposed BVR circuit generates an output voltage of 0.238 V with a temperature coefficient of 58.1 ppm/°C, and the minimum supply voltage is 0.85 V.

3.2 BVR circuits that uses threshold voltage reduction by forward biasing the substrate of the MOSFETs

Another limitation in implementing low voltage CMOS BVR circuits is the threshold voltage that does not scale down as the supply voltage. Leung et al. [19], proposed a CMOS BVR circuit that achieves sub 1 V operation by means of partially forward bias of the PMOS transistors to reduce their threshold voltage. For the BVR circuit shown in Fig. 9(a), the minimum input common mode voltage of an opamp having NMOS input stage is required to be less that one $V_{EB(on)}$ (i.e., $V_{th,n} + 2V_{DS\ (sat)} < V_{EB(on)}$), which implies that transistors with $V_{th,n} < 0.6$ V should be used assuming $V_{EB(on)} = 0.7$ V and $V_{DS\ (sat)} = 0.05$ V. Even though NMOS transistors with $V_{th,n} < 0.6$ V can easily be found in many submicron CMOS technologies, however, the temperature effect on the base-emitter voltage and threshold voltage should be considered. Given that the temperature coefficient of the base-emitter voltage is approximately −2 mV/K while that of threshold voltage of the NMOS transistor may be greater than −2 mV/K, therefore at high temperature $V_{EB(on)}$ may be less than $V_{th,n} + 2V_{DS\ (sat)}$ and the BVR circuit will not function properly. Thus either native transistors or NMOS transistor with $V_{th,n} < 0.5$ V are required to allow the reference circuit to operate down to a single 1-V supply. When the BVR circuit uses opamp having PMOS input stage, as shown in Fig. 9(b), the minimum supply voltage is $V_{EB(on)} + |V_{th,p}| + 2V_{DS\ (sat)}$, and so $|V_{th,p}| < 0.2$ V is required to implement a 1-V reference, which represents a major limitation. To address this limitation, the reference core as proposed by Banba et al. [9], is modified and the input of the opamp is connected to nodes a_1 and b_1 instead of nodes a and b as illustrated in Fig. 10. The opamp enforces voltage at nodes a_1 and b_1 to be equal. As a result voltages at nodes a and b are also equals when $R_{2A_1} = R_{2B_1}$ and $R_{2A_2} = R_{2B2}$. The loop formed by Q_1, Q_2, R_1, R_{2A_1}, R_{2B_1}, R_{2A_2}, and R_{2B_2} generates a current I given by

$$I = \frac{V_{BE}}{R_2} + \frac{V_T \ln(N)}{R_1} \tag{16}$$

where N is the emitter area ratio, V_T is the thermal voltage, and $R_2 = R_{2A_1} + R_{2A_2} = R_{2B_1} + R_{2B_2}$. The current I is injected to R_3 by the current mirror formed by M_1, M_2 and M_3 and gives the reference voltage as follows including the effect of the offset voltage (V_{os}) of the opamp:

$$V_{REF} = \frac{R_3}{R_2}\left[V_{EB_2} + \frac{R_2}{R_1}\left(\ln(N)V_T + \frac{R_2}{R_{2A_2}}V_{OS}\right)\right] \tag{17}$$

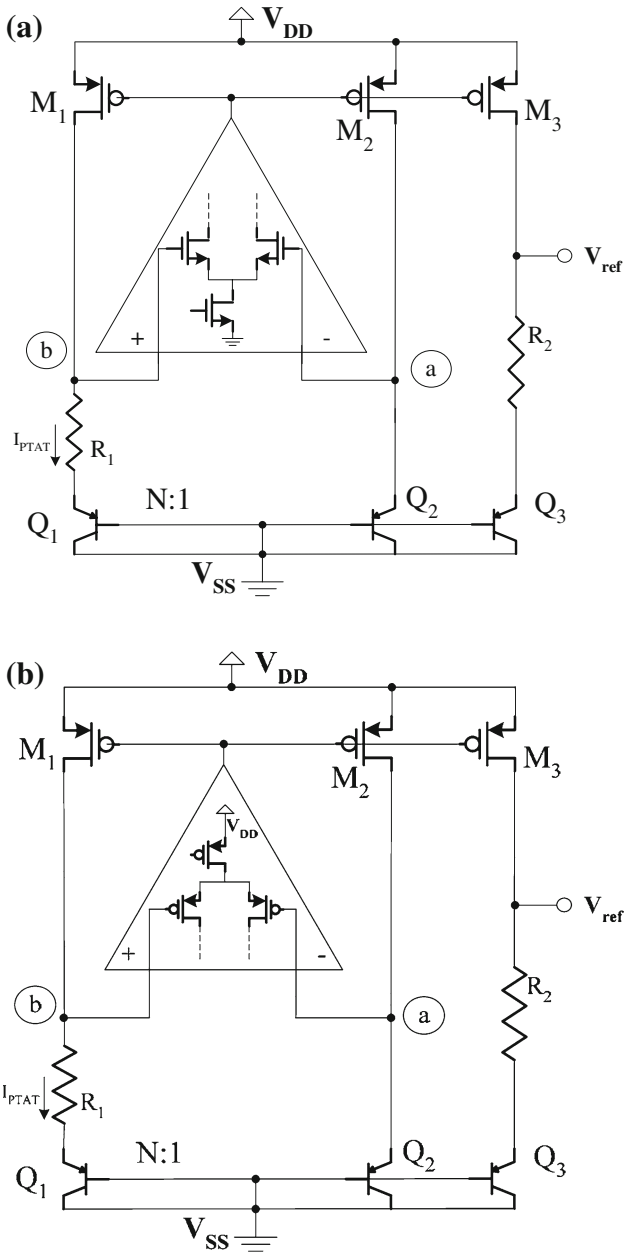

Fig. 9 Bandgap voltage reference in CMOS technology using an amplifier with: **a** NMOS input stage, **b** PMOS input stage, proposed by Leung et al. [11]

A fraction of the material bandgap voltage can be obtained by an appropriate choice of resistor ratio of R_3 to R_2. Moreover, trimming of the resistor ratio of R_1, R_2 to achieve a good TC can be done on R_{2A_1} and R_{2B_1} simultaneously. In addition, in order to minimize the error introduced by the opamp offset voltage, the authors used a larger emitter area ratio ($N = 64$), thus reducing the required resistor ratio of R_1, R_2. The minimum supply voltage is given by

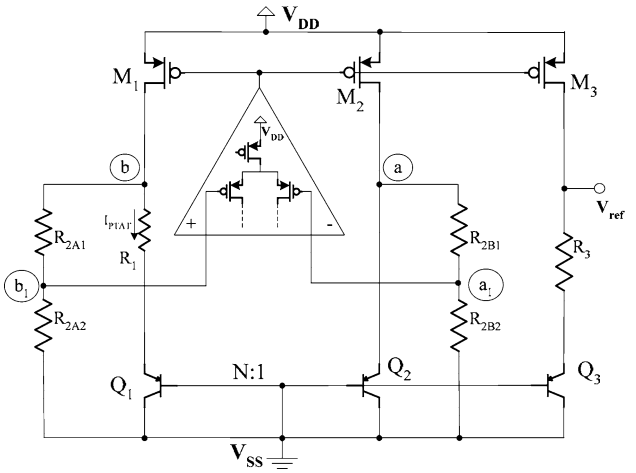

Fig. 10 Sub 1-V bandgap voltage reference in CMOS technology using an amplifier with: PMOS input stage proposed by Leung et al. [11]

$$\min\{V_{DD}\} = \frac{R_{2B2}}{R_{2B1}+R_{2B2}}V_{EB_2} + \left|V_{th,p}\right| + 2\left|V_{DS,(sat)}\right| \tag{18}$$

The proposed BVR circuit architecture achieves an output voltage of 0.630 V with a temperature coefficient of 15 ppm/°C, and the minimum supply voltage is 0.98 V.

Traditionally, CMOS BVR circuits have been based on the use of either vertical PNP or NPN BJT transistors. Given that vertical NPN BJT transistors can be fabricated within standard CMOS process by using a deep N-well structure, Ker et al. [20] proposed a curvature compensation technique for CMOS BVR circuit that combine two BVR circuits which are built by means of the NPN and PNP as illustrated in Fig. 11. Two reference currents I_{REF_1} and I_{REF_2} are generated from the BVR which use PNP and NPN transistors, respectively and are given by:

$$I_{REF_1} = \frac{\left|V_{BE,PNP}\right|}{R_{1,PNP}} + \frac{1}{R_{3,PNP}}\frac{kT}{q}\ln(N_{PNP}) \tag{19}$$

where $R_{1,PNP} = R_{1a,PNP} + R_{1b,PNP}$ (or $R_{2a,PNP} + R_{2b,PNP}$), $R_{1a,PNP} = R_{2a,PNP}$, and $R_{1b,PNP} = R_{2b,PNP}$.

$$I_{REF_2} = \frac{\left|V_{BE,NPN}\right|}{R_{1,NPN}} + \frac{1}{R_{3,NPN}}\frac{kT}{q}\ln(N_{NPN}) \tag{20}$$

where $R_{1,NPN} = R_{1a,NPN} + R_{1b,NPN}$ (or $R_{2a,NPN} + R_{2b,NPN}$), $R_{1a,NPN} = R_{2a,NPN}$, and $R_{1b,NPN} = R_{2b,NPN}$. A temperature independent current I_{REF} is generated by taking the difference between current mirrors formed by $M_{4,PNP}$–$M_{5,PNP}$, and $M_{4,PN}$–$M_{5,NPN}$ and feed into resistor R_{REF} to generate the output voltage V_{REF} given by:

$$V_{REF} = R_{REF}\left[\left(\frac{k_2 V_{BE,NPN}}{R_{1,NPN}} - \frac{k_1\left|V_{BE,PNP}\right|}{R_{1,PNP}}\right) + \frac{kT}{q}\left(\frac{\ln(N_{NPN})}{R_{3,NPN}} - \frac{\ln(N_{PNP})}{R_{3,PNP}}\right)\right] \tag{21}$$

Opamp offset voltage effects would contribute to additional error voltage given by

$$\Delta V_{REF,error} = R_{REF}\left(\frac{k_2 R_{1,NPN}}{R_{1B,NPN}}V_{OS,N} - \frac{k_1 R_{1,PNP}}{R_{1B,PNP}}V_{OS,P}\right) \tag{22}$$

where $V_{OS,N}$, and $V_{OS,P}$, are the offset voltage of the opamp used in the BVR circuit using NPN and PNP BJT, respectively.The effect of $V_{OS,N}$, $V_{OS,P}$, can be reduced by increasing the emitter area ratio of the BJTs (NPN and PNP) and consequently, the required resistance ratio of $k_2 R_{1,NPN}/R_{1b,NPN}$ and $k_1 R_{1,PNP}/R_{1b,PNP}$ would be reduced

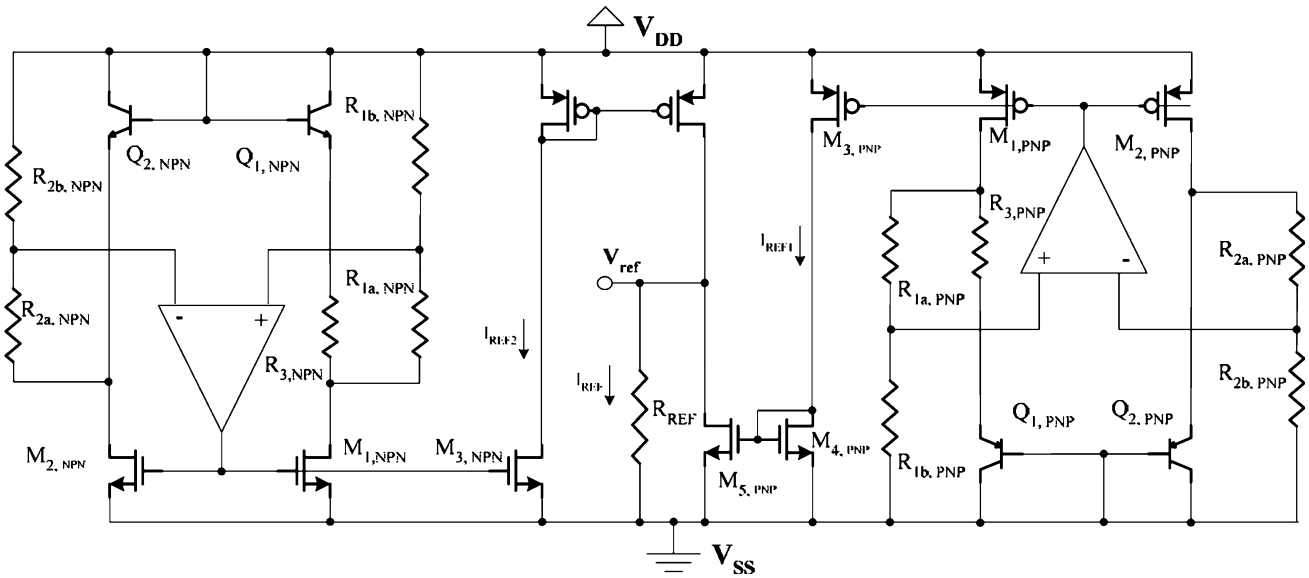

Fig. 11 Curvature compensated a bandgap voltage reference proposed by Ker et al. [20]

to minimize the effect of V_{OS}. The output voltage of the proposed BVR circuit is 0.536 V with a temperature coefficient of 19.5 ppm/°C, and a minimum supply voltage of 0.9 V while consuming 50 μA.

One of the limitations of the BVR circuit proposed by Banba et al., is the opamp common mode voltage requirements. In addition another limitation for the BVR circuit proposed by Malcovati et al., is that BiCMOS technology is more expensive than standard digital CMOS technology process. Boni [21], proposed the opamp circuit illustrated in Fig. 12 intended for sub 1 V BVR circuit implementation. This opamp is a modified version of a standard two stages opamp. The PMOS current mirror load of the input stage is replaced by symmetrical active load driven by a common feedback control. The common mode feedback operation is done by splitting the tail current generator into two identical transistors M_{0A} and M_{0B} having their gate voltages being controlled by the output of the differential stage. The authors implemented several BVR circuits that generate output voltage of 0.493 V.

Doyle et al. [12] proposed a BVR circuit depicted in Fig. 13 that uses PMOS transistors with partially forward bias source bulk PN junction in combination with operation in the subthreshold region. This circuit averages the output voltage with resistors R_3 and R_4 outside of the feedback loop, thus enabling the proposed circuit to be less sensitive to stability problem due to the loading in the feedback loop when using a power-on-reset (POR) circuit. The output voltage of the circuit which is half the output voltage of conventional BVR circuit is given by

$$V_{\mathrm{REF}} = \frac{1}{2}(KV_T \ln(KN) + V_{D_3} - KV_{\mathrm{OS}}) \tag{23}$$

where K is the current ratio of diode connected transistors Q_1 and Q_2, and N is their area ratio. Therefore, by proper choice of the resistor value, the proposed circuit achieves untrimmed output voltage of 0.631 ± 0.020 V, and the output voltage becomes 0.631 ± 0.0015 V after trimming. The temperature coefficient is 17 ppm/°C when the temperature changes from −40 to 125°C, with a current consumption of 10 μA, and a minimum supply voltage of 0.95 V.

Similar technique was used by Ytterdal [22], to demonstrate the implementation of CMOS BVR circuit under a supply voltage of 0.6 V as illustrated in Fig. 14. The BJT transistors used in traditional BVR circuits are replaced by NMOS devices in the weak inversion region, which enables the author to take advantage of the lower voltage drop, and all PMOS source bulk junction are forward biased to reduce their threshold voltage. In addition, the author also uses low threshold voltage NMOS transistors to enhance the operation of the opamp. The reported

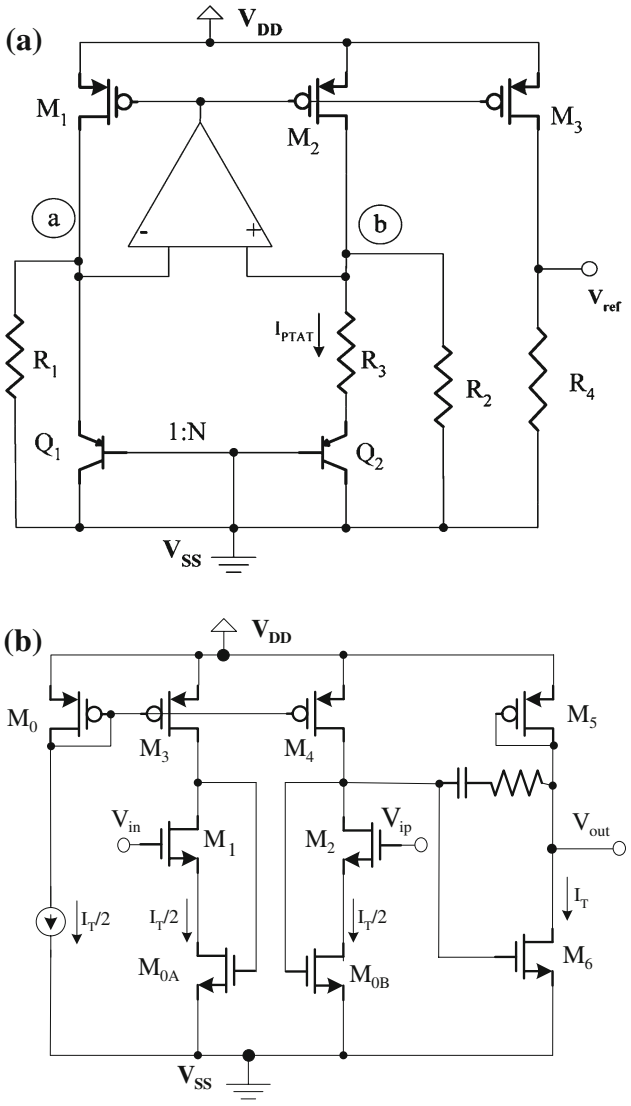

Fig. 12 CMOS-based subthreshold voltage reference proposed by Boni [21]. **a** Low voltage current mode CMOS bandgap reference, **b** opamp for current mode bandgap

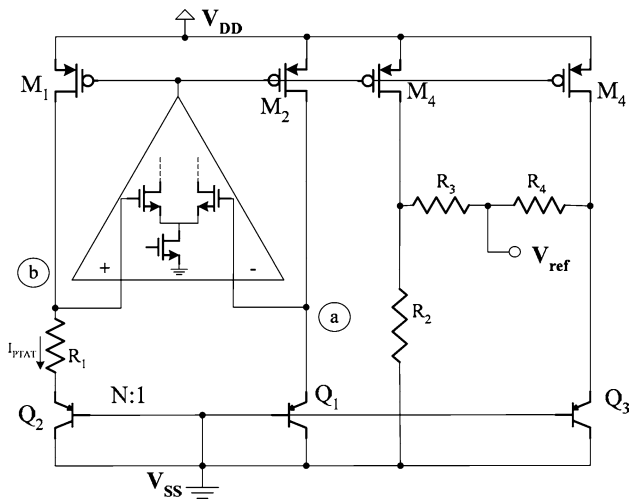

Fig. 13 Bandgap voltage circuit proposed by Doyle et al. [12]

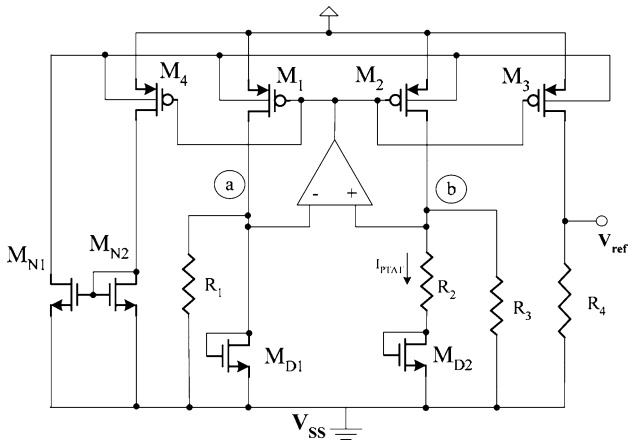

Fig. 14 CMOS-based voltage reference proposed by Ytterdal et al. [22]

simulation results are an output reference voltage of 0.6 V and a temperature coefficient of 93 ppm/°C.

3.3 BVR circuits based on the zero temperature coefficient point

The studies conducted by Filanosky et al. [23], show that under a certain technology-dependent bias point, when biased with a fixed drain current, the gate source voltage of a MOSFET decreases with increasing temperature in a quasi-linear fashion. This is due to the effect of mutual compensation of mobility and threshold voltage effects in CMOS which result in a zero temperature coefficient point (ZTC) in the MOSFET transconductance characteristics.

This technique has been used to realize a sub 1 V CMOS BVR circuit depicted in Fig. 15 [24]. Transistors M_5, M_6 supply PTAT current to the transistors M_7, M_8, respectively, which are operated below the ZTC point. The current I_B is proportional to temperature. All resistors are realized by using N^+ nonsilicide diffusion. The output voltage V_{REF} is given by

$$V_{\mathrm{REF}} = \frac{V_{\mathrm{GS}_7}}{1 + (R_1/R_2)} + \frac{V_{\mathrm{GS}_8}}{1 + (R_1/R_2)} \tag{24}$$

3.4 BVR circuits based on subthreshold MOSFET

The gate source voltage can be used instead of a base-emitter voltage to design a voltage reference independent of temperature. Assuming a long channel MOSFET, and no body effect ($V_{\mathrm{BS}} = 0$), and $V_{\mathrm{DS}} = 4V_T$, the gate source voltage can be expressed as a function of temperature and is given by

$$V_{\mathrm{GS}}(T) \approx V_{\mathrm{GS}}(T_0) + K_{\mathrm{G}}\left(\frac{T}{T_0} - 1\right) \tag{25}$$

where

$$K_{\mathrm{G}} \equiv K_{\mathrm{T}} + V_{\mathrm{GS}}(T_0) - V_{\mathrm{th}}(T_0) - V_{\mathrm{OFF}} \tag{26}$$

and $K_T < 0$ is the temperature coefficient that is used to model the dependence of the threshold voltage over temperature as $V_{\mathrm{th}}(T) = V_{\mathrm{th}}(T_0) + K_{\mathrm{T}}\,(T/T_0 - 1)$.

Giustolisi et al. [13], proposed the voltage reference circuit shown on Fig. 16, based on the operation of MOS transistors in the subthreshold region. The feedback around transistor M_1 forces current I_{R1} to be:

$$I_{R_1} = \frac{V_{\mathrm{GS}_1}}{R_1} \tag{27}$$

This current is copied by M_5 and M_6, and the output voltage is given by

$$V_{\mathrm{REF}} = \alpha V_{\mathrm{GS}_1} + \beta V_{\mathrm{T}} \tag{28}$$

where

$$\begin{aligned} \alpha &= \left(\frac{R_4}{R_3} + 1\right)\frac{R_2 S_5}{R_1 S_4} - \frac{R_4 S_6}{R_1 S_4} \\ \beta &= \left(\frac{R_4}{R_3} + 1\right)\ln\left(\frac{S_8 S_5}{S_7 S_4}\right) \end{aligned} \tag{29}$$

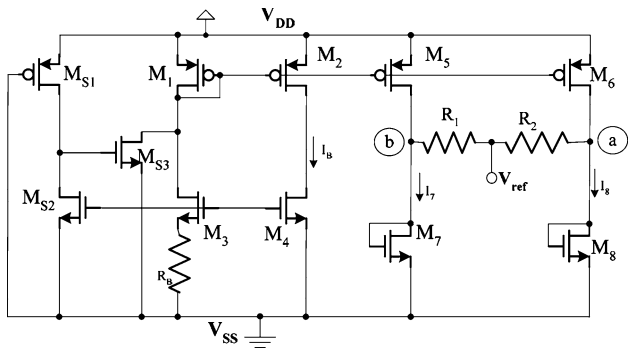

Fig. 15 CMOS-based voltage reference using the zero temperature coefficient point proposed by Najafizadeh et al. [24]

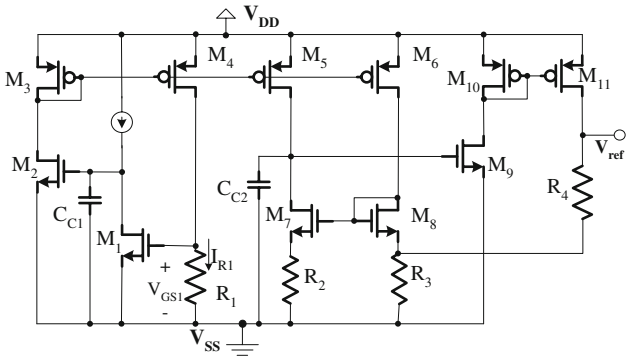

Fig. 16 Subthreshold-based CMOS voltage reference proposed by Giustolisi et al. [13]

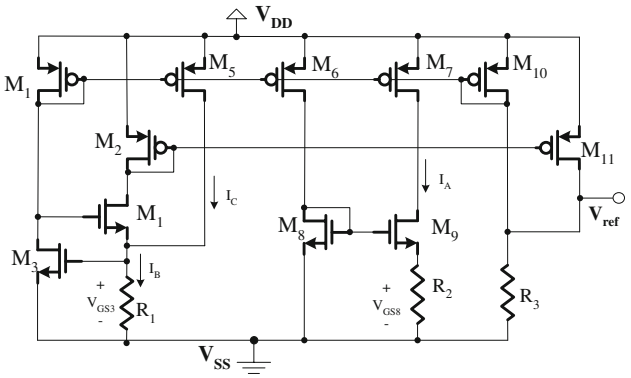

Fig. 17 Subthreshold-based CMOS voltage reference circuit proposed by Huang et al. [25]

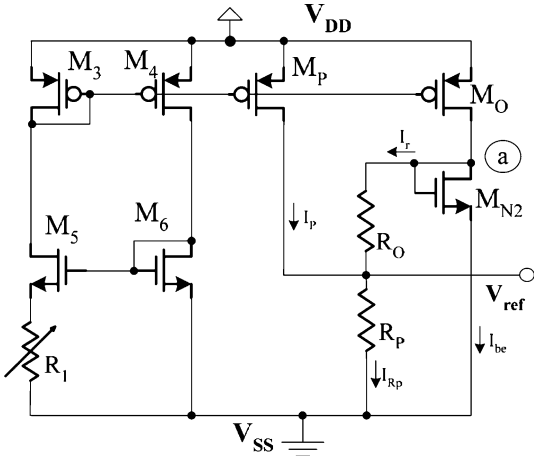

Fig. 18 CMOS voltage reference circuit proposed by Pletersek [26]

where $S = W_{\text{eff}}/L_{\text{eff}}$ is the transistor aspect ratio. The proposed architecture achieves an output voltage of 0.2953 ± 0.0108 V, a temperature coefficient of 119 ± 35.7 ppm/°C when the temperature changes from −25 to 125°C, a voltage supply coefficient of 2 mV/V, and a minimum supply voltage of 1.2 V and a current consumption of 3.6 μA.

Recently, based on the same principle, Huang et al. [25], proposed a simplify version of Giustolisi's BVR circuit as illustrated in Fig. 17. In this circuit, the transistors M_8, and M_9 which operate in the subthreshold region, generate a PTAT current I_{A}. The current I_{A} is mirrored by M_1 to generate V_{GS_3}, and produces a CTAT current I_{B}, with transistor M_3 being operated in the subthreshold region too. Transistor M_5 is used to mirror the current I_{A} and to produce current I_{C} which is N times I_{A}. The transistors M_{10} and M_{11} mirror the current I_{A} and I_{B} respectively to generated the output reference voltage V_{REF} as given below

$$V_{\text{REF}} = \left[\frac{S_{10}}{S_7} I_{\text{A}} + \frac{S_{11}}{S_2}\left(\frac{V_{\text{GS}_3}}{R_1} - N \times I_{\text{A}}\right)\right] \times R_3 \tag{30}$$

where $V_{\text{GS}_3} = \varsigma V_{\text{T}} \ln(I_{\text{D}_3}/I_0)$ and ζ is a non-ideal factor. This outlines the exponential dependence of MOSFET drain current over the gate source voltage when operated in the week inversion region. The proposed architecture achieves an output voltage of 0.221 ± 0.006 V, when the temperature changes from −20 to 120°C, with a voltage supply sensitivity of 2 mV/V, a minimum supply voltage of 0.85 V, and an average power consumption of 3.3 μW.

3.5 BVR circuits based on threshold voltage

Recently, Pletersek [26] proposed a CMOS BVR circuit based on threshold voltage difference across an n-well resistor as illustrated in Fig. 18. The BVR circuit takes advantage of the highly negative PTAT current temperature coefficient produced by the threshold voltage difference. Transistors M_O, M_P and n-well resistors R_O and R_P form the negative PTAT current source. When the voltage at node a (V_a) exceeds a constant reference voltage, the current I_{Rp}, into resistor R_P becomes the sum of current I_P, and I_r that is proportional to V_a, or the drain voltage of transistor M_{N2}. The current difference I_r ($I_r = I_O - I_{\text{be}}$) is regulated by means of the temperature dependency of $V_{\text{GS(MN}_2\text{)}}$ and the temperature dependency of the current I_O. The loop implemented by resistor R_O, achieves the current summation principle. The result of the self-regulated loop is a strongly nonlinear drain bias current with a positive temperature coefficient current. Therefore, a nonlinear current flows through R_P as a result of the voltage difference ($V_a - V_{\text{REF}}$) and by having resistor R_O between the two nodes. The nonlinear correction is achieved by making the drain current I_{be} temperature dependent in such a manner that the nonlinearity in $V_{\text{GS(MN}_2\text{)}}$ (T) is reduced by means of acting the current I_{O} where the resistors temperature coefficients (R_1 and R_0) is included. Consequently, the output voltage becomes nearly constant and is given by

$$V_{\text{REF}} = \frac{V_{\text{BE}}\frac{R_{\text{P}}}{R_0} + \Delta V_{\text{BE}}\frac{R_{\text{P}}}{R_1}}{1 + \frac{R_P}{R_0}} = \text{const} \tag{31}$$

Consequently, as all terms are temperature dependents, the gate source voltage is linearized by the nonlinear increase of the drain current I_{be}.

Ugajin et al. [14], proposed a BVR circuit that sums, respectively the threshold voltages of an enhanced and a depleted mode NMOS and PMOS transistors. The depletion mode PMOS transistor is an undoped PMOS transistor that differs from normal PMOS device only by impurity concentration in the channel region and has the advantage of having a lower threshold voltage. Circuit implementation of the voltage reference, which combine enhancement mode NMOS and depletion mode PMOS transistor, is shown in Fig. 19. Moreover, the mobility behavior of an undoped CMOS/SOI transistor and a normal device are similar. The authors used transistors which have equals

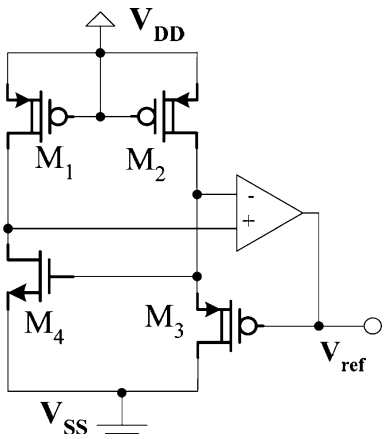

Fig. 19 CMOS/SOI voltage reference circuit proposed by Ugajin et al. [14]

transconductances in order to achieve higher supply voltage insensitivity. In addition, the reference transistors here have been chosen to have exactly opposite temperature dependence of threshold voltage and same temperature dependence of mobility. The authors used a fully depleted CMOS/SIMOX technology, and achieved an output voltage of 0.530 ± 0.0168 V, a temperature coefficient of 0.02 ± 0.06 mV/°C when the temperature changes from 0 to 80°C, and a minimum supply voltage of 0.6 V.

Another example of reference voltage based on the threshold voltage is the work proposed by Ferreira et al. [27]. This reference is similar to one typical Bandgap reference, but instead of generating an output voltage equal to the silicon Bandgap voltage, in this case, the output is equal to the threshold voltage extrapolated to absolute zero Kelvin.

The circuit, shown in Fig. 20, uses only MOS devices working in subthreshold operation, that makes possible low-voltage and low-power operation. The output voltage is given by Eq. 32:

$$V_O(T) = R_2(T) \times I_B(T) + V_{Q_4}(T) \tag{32}$$

As already explained, MOSFET devices in subthreshold operation act similarly as bipolar device and present a gate-source voltage with an almost linear negative dependence with respect of temperature. Thus the CTAT term of Eq. 32 is V_{Q_4}—the gate-source voltage of the diode-connected transistor Q_4. The PTAT term of Eq. 32 is the bias current I_B generated by devices Q_1, Q_2, Q_3 and Q_4, and resistor R_1. The PTAT behavior of I_B comes from the PTAT dependence of drain-source voltage of composite transistors Q_1 and Q_2. Composite transistors are shown in Fig. 21. The drain-source voltage of composite devices is given by Eq. 33, where n is the slope factor in weak inversion. If the PTAT and CTAT terms of Eq. 32 are added in a balanced way, the output voltage is equal to the threshold voltage extrapolated to absolute zero. The authors used a 0.35 μm

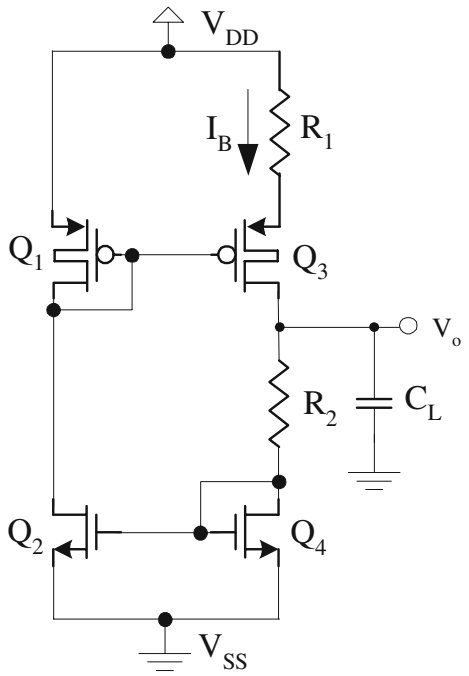

Fig. 20 CMOS Threshold voltage reference source proposed by Ferreira [27]

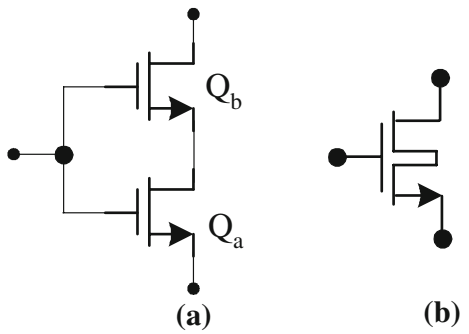

Fig. 21 NMOS composite transistor: **a** schematic and **b** symbol proposed by Ferreira [27]

n-well CMOS process, and achieves an output voltage of 741 mV under just 390 nW for a power supply of 950 mV.

$$V_{\mathrm{DSa}} \approx V_T \times \ln\left(1 + \left(\frac{(W/L)_b}{(W/L)_a}\right)^n\right) \tag{33}$$

3.6 BVR circuits based on gate work function

Traditional BVR circuit design techniques have been focusing on providing a stable voltage reference based on threshold or gate source voltage difference circuits or circuits that are base on emitter voltages difference. The threshold voltage of MOS transistor is given as

$$V_{\text{th}} = \psi_m - \psi_s - \frac{Q}{C_{\text{ox}}} + \frac{2\sqrt{\varepsilon_{\text{si}} q N_a \phi_b}}{C_{\text{ox}}} + 2\phi_b \tag{34}$$

where

$$\psi_m = \frac{1}{q}\left(\chi_{\text{poly-Si}} + \frac{E_{g_{\text{poly-Si}}}}{2}\right) + \phi_{\text{gate}}$$
$$\psi_s = \frac{1}{q}\left(\chi_{\text{Si}} + \frac{E_{g_{\text{Si}}}}{2}\right) + \phi_b \tag{35}$$

$\chi_{\text{poly-Si}}$ and χ_{Si} are electron affinities of poly-Si and Si. $E_{g_{\text{poly-Si}}}$ and $E_{g_{\text{Si}}}$ are bandgaps of poly-Si and Si respectively. For a pair of transistors with gate impurities of opposite conductivity types, having concentrations of p^+ and n^+, the V_{th} difference V_{pn} is given by

$$V_{\text{pn}} = \frac{kT}{q}\ln\frac{N_{p^+}N_{n^+}}{N_i^2} \tag{36}$$

For a pair of transistors with gate impurities of opposite conductivity types, having concentrations of p^+ and n^+, the V_{th} difference V_{pn} is given by

$$V_{\text{nn}} = \frac{kT}{q}\ln\frac{N_{n^+}}{N_{n^-}} \tag{37}$$

Watanabe et al. [15], proposed a sub 1 V CMOS BVR circuit illustrated in Fig. 22 composed of NMOS transistors built in separate p-wells and having different gate impurities concentration. The BVR circuit is composed of a circle device M_2, with p^+ gate; a triangle device M_4, with n^- gate and all others devices have n^+ gate type. Transistor M_1 is used as a depletion mode transistor and acts as a current source. The output reference voltage is given by

$$V_{\text{REF}} = \frac{R_2}{R_1 + R_2}V_{\text{pn}} + V_{\text{nn}} \tag{38}$$

The proposed BVR circuit achieves an output voltage of 0.41 ± 0.0082 V, a temperature coefficient of 80 ppm/°C when the temperature changes from −50°C to 100°C, and the minimum supply voltage is 1 V with a current consumption of 0.6 μA.

3.7 BVR circuits based on virtual/real low-bandgap devices

Operation of BVR circuit below the material bandgap has become mandatory for next generation of consumers electronics products, upcoming electronics devices and systems. The design techniques that have been proposed are based on the generation of a fraction of the material bandgap but at the expense of extra area required for additional resistors. Alternate design technique proposed by Annema [16], consists of lowering the material bandgap by increasing the electrostatic field across the junction. There is a built-in voltage Φ_{GW} between the gate and well due to the presence of P-type gate over the N-type well. This built-in voltage is subdivided over the gate oxide and over the silicon due to capacitive division. The resulting voltage drop in the silicon is given by

$$\phi_{b_1} = \frac{\Phi_{\text{GW}} C_{\text{ox}}}{C_{\text{ox}} + C_{\text{depletion}}(\phi_{b_1})} \tag{39}$$

where

$$\Phi_{\text{GW}} \cong V_{\text{gap}} + \frac{kT}{q}\ln\left(\frac{N_{\text{well}}}{N_c N_v}\right) + \Delta V \tag{40}$$

and N_c, N_v are temperature dependent densities of states in the conductance band and valance band respectively. ΔV accounts for additional effects such as bandgap differences between monosilicon (well material) and polysilicon (gate material), bandgap narrowing, and fixed oxide charges.

Consequently, for DTMOS transistors based diode, due to their gate-to-body tied structure, the applied gate voltage would result in an increased of the electrostatic field across the junction, and the effective bandgap voltage becomes

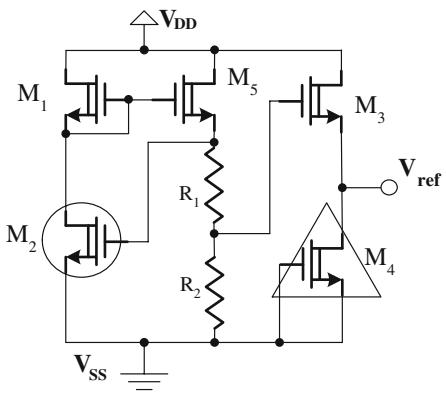

Fig. 22 CMOS voltage reference based on N-channel MOSFETs gate work function difference proposed by Watanabe et al. [15]. Circle indicates p^+ gate, triangle indicates n^- gate, all others are n^+ gate

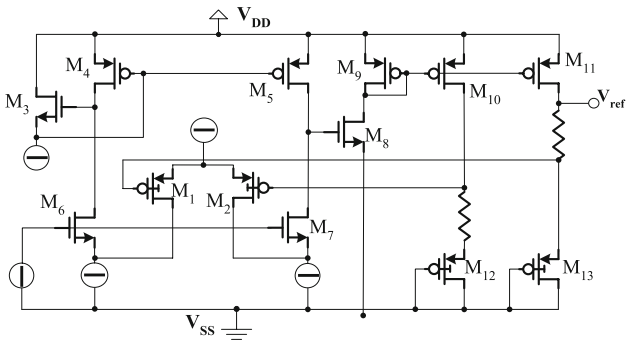

Fig. 23 DTMOS-based voltage reference based proposed by Annema [16]

Table 1 Performance summary sub 1-V bandgap voltage reference circuits design techniques

BVR circuit	V_{REF} (V)	Minimum supply voltage (V)	Temperature range (°C)	Technology process	Temperature coefficient	Supply current (μA)	Chip area (mm^2)	ΔV_{REF} due to ΔV_{DD} (mV)	ΔV_{REF} due to Δtemp (mV)
Jiang et al. [1]	1	1.2	0 to 100	CMOS 1.2 μm	–	500	–	–	10
Neuteboom et al. [8]	0.670	0.7	–	CMOS[a] 0.8 μm	–	20	0.15	–	–
Banba et al. [9]	0.515	2.1	27 to 125	CMOS[b] 0.4 μm	–	2	–	±1	±3
Malcovati et al. [10]	0.536	1	0 to 80	BiCMOS 0.8 μm	7.5 ppm/K	92	0.25	0.114	0.3
Kim [28]	0.670	1	5 to 56	0.18 μm Si CMOS	287 ppm/°C	–	–	–	9.3
Ker et al. [11]	0.238	0.85	−10 to 120	CMOS 1.2 μm	58.1 ppm/°C	28	–	–	–
Leung et al. [19]	0.603	0.98	0 to 100	CMOS 0.6 μm	15 ppm/°C	18	0.24	2.2	–
Andrea Boni [21]	0.493	1	−40 to 140	CMOS 0.35 μm	–	–	–	–	–
		1.5		CMOS 0.35 μm	–	–	–	2	2.5 when $V_{DD} = 1.2$ V
		–		CMOS 0.18 μm	–	–	–	6.5	1.5 when $V_{DD} = 1.8$ V
		0.85		CMOS 0.35 μm	–	–	–	–	–
Ker et al. [20]	0.536	0.9	0 to 100	CMOS 0.25 μm	19.5 ppm/°C	50	0.108	10	2
Doyle [12]	0.631	0.95	−40 to 125		17 ppm/°C	10	1.06	–	20, untrimmed 1.5 after trimming
Ytterdal [22]	0.400	0.6	−40 to 100	CMOS* 0.13 μm	93 ppm/°C	–	–	–	–
Giustolisi et al. [13]	0.295	1.2	−25 to 125	CMOS 1.2 μm	119 ppm/°C	3.8		–	10.8
Huang et al. [25]	0.221	0.85	−20 to 120	CMOS 0.18 μm	–	3.3	0.0238	2	6
Pletersek [26]	0.356	0.8	−50 to 160	CMOS 0.6 μm	–	2.5	0.04	–	20, untrimmed 3, after trimming
Ugajin et al. [14]	0.530 ± 0.0168	0.6	–	–	0.02 ± 0.06 mV/°C	100	0.06	–	–
Watanabe [15]	0.410	1	−50 to 100	–	80 ppm/°C	0.6	–	–	7
Ferreira [27]	0.741	0.95	−20 to 80	CMOS 0.35 μm	39 ppm/°C	0.25	0.0759	–	4
Annema [16]	0.65	0.85	−20 to 100	CMOS 0.35 μm	–	1.2	0.063	–	4.5, untrimmed

[a] Using a low threshold voltage CMOS process

[b] Reported for the standard CMOS process, simulations showed that $V_{DD} = 0.85$ V is feasible in combination with a low V_{th} process

$$V_{\text{gap,effective}} = V_{\text{gap,0}} - \phi_{b_1} \quad (41)$$

which is temperature dependent. This effective bandgap extrapolated to 0 K is about 0.6 V, which is half that of standard bipolar transistor and diode in silicon. The circuit proposed by Annema is shown in Fig. 23, where M_1 and M_2 are DTMOS transistors used in the input stage of the opamp circuit, M_{12} and M_{13} are DTMOS-based diodes with lower bandgap voltage. The BVR circuit generates and output voltage of 0.65 V under a minimum supply voltage of 0.85 V while consuming 1.2 μA of current.

Another way to decrease the supply voltage requirements is using Ge (Germanium diodes) whose bandgap voltage is only 0.6 V (half of silicon). Kim [28] proposed a hybrid BVR using integrated devices and discrete Ge diodes to achieve an output voltage of 670 mV with a variation of 9.3 mv (ppm/°C). This reference presents the same topology presented by Fig. 2, however the BJTs are replaced by Ge diodes.

One drawback of this circuit is the limited temperature range of operation. It was demonstrated that the lower limit of the Ge diode voltage is about three times the thermal voltage, and below this value, the temperature performance of the output voltage is degraded. Due to this issue, the highest temperature operation used in that work is 56°C. Besides this limitation, the use of discrete diodes does not comply with the current trend of ultra-integration. It is evident that discrete diodes can be replaced by integrated devices, but this option is very expensive.

4 Summary

CMOS voltage reference is a pivotal building in analog circuit design. A detailed summary on the state-of-the-art BVR circuit is given in Table 1. We have provided an in-depth survey of the existing sub 1 V BVR circuit design techniques, which give insights a designer can relay upon when building CMOS voltage reference.

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